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EXAMINER	
MCCLOUD, RENATA D	
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2837	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/988,439	KIKUCHI, AKITOSHI	
	Examiner	Art Unit	
	Renata McCloud	2837	AU

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1- 56 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

Claims 1 and 16: The limitation "N (in number)" is unclear. What does "in number" mean? The limitation "until at least next synchronous signal is reached" is unclear. There appears to be a grammatical error here.

Claims 10 and 38: The limitation "N (in number)" is unclear. What does "in number" mean? The limitation "reading an image with line unit" appears to have a grammatical error. The limitation "acceleration/deceleration" is unclear. Does this mean both "acceleration and deceleration", or either "acceleration or deceleration"?

Claim 40: recites the limitation "said reading restart instructing means". There is insufficient antecedent basis for this limitation in the claim. The term "sufficient" is a relative term which renders the claim indefinite. The term "sufficient" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite

degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claims 3, 6, 18, 22, 27, 28, 31, 35, 46, 50, 55, 56: The limitation "acceleration/deceleration" is unclear. Does this mean both "acceleration and deceleration", or either "acceleration or deceleration"?

Claims 4, 13, 29, 32: The limitation "N (in number)" is unclear. What does "in number" mean?

Claim 12: recites the limitation "said reading re-start instructing means". There is insufficient antecedent basis for this limitation in the claim.

Claim 25: the limitation "a predetermined the number of bits" is unclear.

Claim 36, 37, 42, 43, 51, and 52: the limitation "in case of an image" is unclear. There appears to be some grammatical errors.

Claim 44: The limitation "N (in number)" is unclear. What does "in number" mean? The limitation "reading an image with line unit" appears to have a grammatical error.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 16, 17, 29, 30, 44, and 45 are rejected under 35 U.S.C. 102(b) as being anticipated by Thompson (US 5,109,476).

Claims 1 and 29: an apparatus and method comprising synchronous signal generating means (Fig. 1:10) generating a synchronous signal (Col. 4:13-19) having a period corresponding to N times of one line of an image (Col. 1:25-32, 5: 16-23; see Claim 5); line trigger producing means (Fig. 1:20) producing N line triggers in synchronous with generation of the synchronous signal (Col. 4:13-24); a motor controller (Fig. 1: 14) controlling a stepping motor (Fig. 3:38); and a CPU (Fig. 1:12) controlling the motor controller (Fig. 1:14) in synchronous with the generation of the synchronous signal (Col. 2: 63-3:5), wherein the motor controller effects motor control until at least a next synchronous signal is reached on the basis of the line triggers (3:25-42).

Claims 16 and 44: an apparatus and method comprising synchronous signal generating means (Fig. 1:10) generating a synchronous signal (Col. 4:13-19) having a period corresponding to N times of one line of an image (Col. 1:25-32, 5: 16-23; see Claim 5); line trigger producing means (Fig. 1:20) producing N line triggers in synchronous with generation of the synchronous signal (Col. 4:13-24); a motor controller (Fig. 1: 14) controlling a stepping motor (Fig. 3:38); and means for receiving instructions (Fig. 1: 10) from a CPU (Fig. 1:12) controlling the motor controller (Fig. 1:14) in synchronous with the generation of the synchronous signal (Col. 2: 63-3:5), wherein the motor controller effects motor control until at least a next synchronous signal is reached on the basis of the line triggers (3:25-42).

Claims 2, 17, 30, and 45 (apparatuses and methods): the motor controller includes first memory means (Fig. 1: 20) holding the timer data advancing a phase of the motor (Col. 3:16-19) and second memory means (Fig. 1:28) for holding the number of steps of the timer data (Col. 3:25-34), the stepping motor is controlled on the basis of the timer data and the number of steps (Col. 3:25-34, 4:20-25).

5. Claims 10, 26, 38, and 54 are rejected under 35 U.S.C. 102(b) as being anticipated by DiBello et al (US 5,992,318).

Claims 10 and 38: an apparatus and method comprising: means for reading an image (Fig. 2.1:52); means for storing the read image (Col. 6: 50-55); means for generating a synchronous signal (Col. 7: 27-29) having a period corresponding to N times of one-line of the image (Col. 7: 44-55); means for producing N line triggers in synchronous generation of the synchronous signal (Col. 7:56-60); a motor control unit (Fig. 2.1: 55) effecting acceleration or deceleration control of the stepping motor on the basis of the line triggers (Col. 23:12-25); a CPU (Fig. 2.1:56) controlling the motor control unit (Fig. 2.1:55) in synchronous with the generation of the synchronous signal (Col. 5:55-57); means for judging a usage state of the storage means; and means for causing the CPU to effect control for stopping the motor with respect to the control unit in synchronous with the generation of the synchronous signal when the judge means judges that vacant capacity of the storing means is smaller than a predetermined value

or that usage amount of the storage means is smaller than a predetermined value (Col. 14: 7-34); wherein the control unit effects stop control for decelerating and stopping the motor on the basis of the line triggers by means of the stop control means (Col. 23:13-45).

Claims 26 and 54: the motor control unit includes means for holding PWM output data having a predetermined number of bits (Col. 6: 30-41) for determining an exciting current for the stepping motor (Col. 7:44-55), and means for outputting the PWM data stored in the PWM output data storing means (Col. 17: 46-50, signal is output through port) synchronous with the stepping motor (Fig. 3.3b), wherein the motor is controlled by setting the number of bits of the PWM data outputted from the PWM output means (Fig. 3:3b).

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
> **(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.**

7. Claim 4, 5, 8,9 and 19, 20 23, 24, 32, 33, 36, 37, 47, 48, 51, 52 are rejected under 35 U.S.C. 102(e) as being anticipated by Nagasawa et al (US 6,384,928).

Claims 4 and 32: an apparatus and method comprising : synchronous signal generating means (Col. 2:17-21); a motor control unit (Fig. 2: 2) controlling the motor (Fig. 2:15 is a disk drive); a CPU (Fig. 2: 22) controlling the motor control unit; and line

trigger means producing N line triggers (Fig. 5; Col. 4:49-61, teaches packets having header fields), wherein the motor control unit has a synchronous mode for controlling the motor in synchronous generation of the synchronous signal (Col. 2:17-21) and a non-synchronous mode (Fig. 4; Col. 4:21-22) for controlling the motor regardless of the generation of the synchronous signal (Col. 4:62-5:7), when the synchronous mode is selected the motor control synchronous with the synchronous signal is effected (Fig. 8; Col. 6:7-18), and when the non-synchronous mode is set, the line trigger means generates line triggers not synchronous with the synchronous signal (Col. 4: 62-67, the node ignores all other packets) and the motor control unit controls the motor on the basis of the line triggers which are not synchronous with the synchronous signal (Col. 5: 7-14, teaches the controller uses asynchronous transfer at start-up, asynchronous is not synchronous).

Claim 19: an apparatus comprising : synchronous signal generating means (Col. 2:17-21); a motor control unit (Fig. 2: 2) controlling the motor (Fig. 2:15 is a disk drive); means for receiving instructions (Fig. 2:23) from a CPU (Fig. 2: 22); and line trigger means producing N line triggers (Fig. 5; Col. 4:49-61, teaches packets having header fields), wherein the motor control unit has a synchronous mode for controlling the motor in synchronous generation of the synchronous signal (Col. 2:17-21) and a non-synchronous mode (Fig. 4; Col. 4:21-22) for controlling the motor regardless of the generation of the synchronous signal (Col. 4:62-5:7), when the synchronous mode is selected the motor control synchronous with the synchronous signal is effected (Fig. 8; Col. 6:7-18), and when the non-synchronous mode is set, the line trigger means

generates line triggers not synchronous with the synchronous signal (Col. 4: 62-67, the node ignores all other packets) and the motor control unit controls the motor on the basis of the line triggers which are not synchronous with the synchronous signal (Col. 5: 7-14, teaches the controller uses asynchronous transfer at start-up, asynchronous is not synchronous).

Claim 47: a method comprising: receiving a synchronous signal (Col. 2:17-21); a motor control unit (Fig. 2: 2) controlling the motor (Fig. 2:15 is a disk drive); receiving control instructions from a CPU (Fig. 2: 11) by the instruction receiving means (Fig. 2:2; Col. 4:17-20); and line trigger means producing N line triggers (Fig. 5; Col. 4:49-61, teaches packets having header fields), wherein the motor control unit (Fig. 2: 2) has a synchronous mode for controlling the motor in synchronous generation of the synchronous signal (Col. 2:17-21) and a non-synchronous mode (Fig. 4; Col. 4:21-22) for controlling the motor regardless of the generation of the synchronous signal (Col. 4:62-5:7), when the synchronous mode is selected , the instruction receiving means (Fig. 2:2) receives the motor control instruction from the CPU (Fig. 2: 11) in synchronous with the synchronous signal (Fig. 8; Col. 6:7-18) and the motor control unit (Fig. 2: 2) effects the motor control on the basis of the instruction (Fig. 3; Col. 4:10-16) received by the instruction receiving means (Fig. 2:2), and when the non-synchronous mode is set, the line trigger means generates line triggers not synchronous with the synchronous signal (Col. 4: 62-67, the node ignores all other packets) and the motor control unit controls the motor on the basis of the line triggers which are not

synchronous with the synchronous signal (Col. 5: 7-14, teaches the controller uses asynchronous transfer at start-up, asynchronous is not synchronous).

Claims 5, 20, and 33: the synchronous signal generating means generates a signal having a period corresponding the N times of one-line of an image (Fig. 5; Col. 4:49-61, teaches packets having header fields), and when the synchronous mode is selected, the line trigger producing means (Fig. 5; Col. 4:49-61, teaches packets having header fields) produces the line trigger synchronous with the synchronous signal (Fig. 8; Col. 6:7-18), and the motor control unit effects motor control until at least next synchronous signal is reached on the basis of the line trigger (Fig. 8; Col. 6:7-18).

Claim 8, 23, 36, and 51: the apparatus of claims 4, 5, 19, 32, 33, and 47, wherein a synchronous mode is selected in the case of an image having great memory usage (Col. 7: 42-61) and the non-synchronous mode is selected in the case of an image having a small memory usage (Col. 7: 21-35).

Claim 9, 24, 37, and 52: the apparatus of claims 4, 5,19, 32, 33, and 47 wherein the synchronous mode is selected in a case of a color image (Col. 7:42-48) and the non-synchronous mode is selected in case of a monochromatic image (Col. 7: 21-35).

Claim 48: the synchronous signal receiving means (Fig. 2:2) receives a signal having a period corresponding the N times of one-line of an image (Fig. 5; Col. 4:49-61, teaches packets having header fields), and when the synchronous mode is selected, the line trigger producing means (Fig. 5; Col. 4:49-61, teaches packets having header fields) produces the line trigger synchronous with the synchronous signal (Fig. 8; Col.

6:7-18), and the motor control unit effects motor control until at least next synchronous signal is reached on the basis of the line trigger (Fig. 8; Col. 6:7-18).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3, 18, 27/3, 27/18, 31, 46, 55/31, and 55/46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson as applied to claim 1, 17, 30, 31, 45, and 46, and further in view of Huang (US 6,388,415).

Claims 3, 18, 31, 46 (apparatuses and methods): Thompson teaches the limitations of claims 1, 17, 30, and 45. Referring to claims 3, 18, 31, and 46, Thompson does not teach the motor controller is synchronized with the line triggers produced by the producing means and controls acceleration and deceleration of the stepping motor by switching acceleration and deceleration tables comprised of the timer data and the number of steps. Huang teaches the motor controller is synchronized with the line triggers produced by the producing means (Col. 4: 5-6) and controls acceleration and deceleration of the stepping motor (Col. 4: 61-62) by switching acceleration and deceleration tables (Fig. 10 show switching of acceleration and deceleration) comprised of the timer data and the number of steps (Col. 7:66-8:24).

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the apparatus taught by Thompson to include tables as taught by Huang. The advantage of this would be the ability to change acceleration and deceleration period without influencing constant speed control.

Claims 27/3, 27/18, 55/31, and 55/46: Thompson and Huang teach the limitations of claims 3,18, 31, and 46. Referring to claims 27/3, 27/18, 55/31/, and 55/46 Huang teaches the motor control unit (Fig. 13: 136) includes step-up or step-down number storing means (Fig. 1: 138) for holding a step-number or a step-down number of the acceleration or deceleration table (Col. 5: Table 1), and step-up or step-down of the acceleration or deceleration table is effected on the basis of the step number or the step-down number held by a step-up or step-down number storing means (Fig. 10).

10. Claims 6, 7, 21, 22, 34, 35, 49, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagasawa et al as applied to claim 4 above, and further in view of Thompson.

Claims 6, 21, 34, and 49: Nagasawa et al teach the limitations of claims 4, 19, 32, and 47. Referring to claims 6, 21, 34, and 49 they do not teach the motor controller includes first memory means holding the timer data advancing a phase of the motor and second memory means for holding the number of steps of the timer data, the stepping motor is controlled on the basis of the timer data and the number of steps. Thompson teaches a motor controller includes first memory means (Fig. 1: 20) holding the timer

data advancing a phase of the motor (Col. 3:16-19) and second memory means (Fig. 1:28) for holding the number of steps of the timer data (Col. 3:25-34), the stepping motor is controlled on the basis of the timer data and the number of steps (Col. 3:25-34, 4:20-25).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus taught by Nagasawa et al to include memory as taught by Thompson. The advantage of this would be ability have enough data available so that there is little wait time for additional data.

Claims 7, 22, 35, and 50: Nagasawa et al and Thompson teach the limitations of claims 6, 21, 34, and 49. Referring to claims 7, 22, 35, and 48, Thompson teaches the motor controller is synchronized with the line triggers produced by the producing means (Col. 4: 5-6) and controls acceleration and deceleration of the stepping motor (Col. 4: 61-62) by switching acceleration and deceleration tables (Fig. 10 show switching of acceleration and deceleration) comprised of the timer data and the number of steps (Col. 7:66-8:24).

11. Claims 13-15, and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over DiBello et al as applied to claims 10 above, and further in view of Nagasawa et al.

Claims 13 and 41: DiBello et al teach the limitations of claims 10 and 38, and referring to claims 13 and 41, the motor control unit has a synchronous mode for

controlling the motor in synchronous generation of the synchronous signal (Col. 7:56-60) and a non-synchronous mode for controlling the motor (Col. 23:55-24:5). They do not teach a non-synchronous mode for controlling the motor regardless of the generation of the synchronous signal, when the synchronous mode is selected, the instruction receiving means receives the motor control instruction from the CPU in synchronous with the synchronous signal and the motor control unit effects the motor control on the basis of the instruction received by the instruction receiving means, and when the non-synchronous mode is set, the line trigger means generates line triggers not synchronous with the synchronous signal and the motor control unit controls the motor on the basis of the line triggers which are not synchronous with the synchronous signal. Nagasawa et al teach wherein the motor control unit (Fig. 2: 2) has a synchronous mode for controlling the motor in synchronous generation of the synchronous signal (Col. 2:17-21) and a non-synchronous mode (Fig. 4; Col. 4:21-22) for controlling the motor regardless of the generation of the synchronous signal (Col. 4:62-5:7), when the synchronous mode is selected, the instruction receiving means (Fig. 2:2) receives the motor control instruction from the CPU (Fig. 2: 11) in synchronous with the synchronous signal (Fig. 8; Col. 6:7-18) and the motor control unit (Fig. 2: 2) effects the motor control on the basis of the instruction (Fig. 3; Col. 4:10-16) received by the instruction receiving means (Fig. 2:2), and when the non-synchronous mode is set, the line trigger means generates line triggers not synchronous with the synchronous signal (Col. 4: 62-67, the node ignores all other packets) and the motor control unit controls the motor on the basis of the line triggers which are not synchronous with the

synchronous signal (Col. 5: 7-14, teaches the controller uses asynchronous transfer at start-up, asynchronous is not synchronous).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus taught by DiBello et al to have synchronous and non-synchronous modes as taught by Nagasawa et al. The advantage of this would be improvement in the performance and functions of the apparatus due the ability to selectively use each mode.

Claims 14 and 42: DiBello et al and Nagasawa et al teach the limitations of claims 13 and 41. Referring to claims 14 and 42, Nagasawa et al teach a synchronous mode is selected in the case of an image having great memory usage (Col. 7: 42-61) and the non-synchronous mode is selected in the case of an image having a small memory usage (Col. 7: 21-35).

Claims 15 and 43: DiBello et al and Nagasawa et al teach the limitations of claims 13 and 41. Referring to claims 15 and 43, Nagasawa et al teach the apparatus of claims 4 and 19 wherein the synchronous mode is selected in a case of a color image (Col. 7:42-48) and the non-synchronous mode is selected in case of a monochromatic image (Col. 7: 21-35).

12. Claims 25/4, 25/16, 53/29, and 53/44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagasawa et al as applied to claims 4, 19, 29, and 44 above, and further in view of DiBello et al.

Claims 25/4, 25/19, 53/29 and 53/44: Nagasawa et al teach the limitations of claims 4, 19, 29, and 44. Referring to claims 25/4, 25/19, 53/29, and 53/44, they do not teach the motor control unit includes means for holding PWM output data having a predetermined number of bits for determining an exciting current for the stepping motor, and means for outputting the PWM data stored in the PWM output data storing means synchronous with a phase of the stepping motor, wherein the motor is controlled by setting the number of bits of the PWM data outputted from the PWM output means. DiBello et al teach the motor control unit includes means for holding PWM output data having a predetermined number of bits (Fig. 3.3) for determining an exciting current for the stepping motor (Col. 7:44-55), and means for outputting the PWM data stored in the PWM output data storing means (Col. 17: 46-50, signal is output through port) synchronous with the stepping motor (Fig. 3.3b), wherein the motor is controlled by setting the number of bits of the PWM data outputted from the PWM output means (Fig. 3.3b).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus taught by Nagasawa et al to use PWM data as taught by DiBello et al. The advantage of this would be reduced image distortion.

13. Claims 25/1, 25/16, 53/32, and 53/47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson as applied to claims 1 and 16 above, and further in view of DiBello et al.

Claim 25/1, 25/16, 53/32, and 53/47: Thompson teaches the limitations of claims 1, 16, 32, and 47. Referring to claims 25/1, 25/16, 53/32, and 53/47, Thompson does not teach the motor control unit includes means for holding PWM output data having a predetermined number of bits for determining an exciting current for the stepping motor, and means for outputting the PWM data stored in the PWM output data storing means synchronous with a phase of the stepping motor, wherein the motor is controlled by setting the number of bits of the PWM data outputted from the PWM output means. DiBello et al teach the motor control unit includes means for holding PWM output data having a predetermined number of bits (Col. 6: 30-41) for determining an exciting current for the stepping motor (Col. 7:44-55); and means for outputting the PWM data stored in the PWM output data storing means (Col. 17: 46-50, signal is output through port) synchronous with the stepping motor (Fig. 3.3b), wherein the motor is controlled by setting the number of bits of the PWM data outputted from the PWM output means (Fig. 3.3b).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus taught by Thompson to use PWM data as taught by DiBello et al. The advantage of this would be reduced image distortion.

14. Claims 26, 28, and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over DiBello et al as applied to claim 10 above, and further in view of Huang.

Claims 26: DiBello et al teach the limitations of claim10. Referring to claim 26, they do not teach motor control unit includes step-up or step-down number storing means for holding a step-number or a step-down number of the acceleration or deceleration table, and step-up or step-down of the acceleration or deceleration table is effected on the basis of the step number or the step-down number held by a step-up or step-down number storing means. Huang teaches a motor control unit (Fig. 13: 136) includes step-up or step-down number storing means (Fig. 1: 138) for holding a step-number or a step-down number of the acceleration or deceleration table (Col. 5: Table 1), and step-up or step-down of the acceleration or deceleration table is effected on the basis of the step number or the step-down number held by a step-up or step-down number storing means (Fig. 10).

Claim 28: DiBello et al and Huang teach the limitations of claim 26, referring to claim 28, Huang teaches a motor control unit (Fig. 13: 136) includes step-up or step-down number storing means (Fig. 1: 138) for holding a step-number or a step-down number of the acceleration or deceleration table (Col. 5: Table 1), and step-up or step-down of the acceleration or deceleration table is effected on the basis of the step number or the step-down number held by a step-up or step-down number storing means (Fig. 10).

Claim 56: DiBello et al teach the limitations of claim 54, referring to claim 56, DiBello et al do not teach a motor control unit includes step-up or step-down number storing means for holding a step-number or a step-down number of the acceleration or deceleration table, and step-up or step-down of the acceleration or deceleration table is

effected on the basis of the step number or the step-down number held by a step-up or step-down number storing means. Huang teaches a motor control unit (Fig. 13: 136) includes step-up or step-down number storing means (Fig. 1: 138) for holding a step-number or a step-down number of the acceleration or deceleration table (Col. 5: Table 1), and step-up or step-down of the acceleration or deceleration table is effected on the basis of the step number or the step-down number held by a step-up or step-down number storing means (Fig. 10).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus taught by DiBello et al to include the teaching of Huang. The advantage of this would be the ability to change acceleration and deceleration period without influencing constant speed control.

15. Claims 39 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over DiBello et al as applied to claim 38 above, and further in view of Yamada (US 6,009,215).

Claim 39: DiBello et al teach the limitations of claim 38. Referring to claim 39, they do not teach means for restarting reading when a vacant capacity of the storing means is greater than a predetermined amount. Yamada teaches means for restarting reading when memory becomes available (Col. 11: 8-24-43).

Claim 40: DiBello et al teach the limitations of claim 38. Referring to claim 40, they do not teach when restarting, the motor control unit accelerates the motor to reversely rotate the motor up to a position to effect speed driving to a position from

which deceleration is started by a stop instruction. Yamada teaches when restarting, the motor control unit accelerates the motor to reversely rotate the motor up to a position to effect speed driving to a position from which deceleration is started by a stop instruction (Col. 10:49-11:43).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus taught by DiBello et al to include the restarting as taught by Yamada. The advantage of this would be prevention of an image disturbance such as positional deviation.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. They are: Ng (US 5,177,507), McFarland et al (US 3,657,707), Fulton et al (US 4,962,393).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renata McCloud whose telephone number is (571) 272-2069. The examiner can normally be reached on Mon.- Fri. from 8 am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Nappi can be reached on (571) 272-2800 ext. 37. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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